REMARKS

Claims 1-195 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-5, 8-16, and 19-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Liu et al. (U.S. Pub. No. 2005/0005044). This rejection is respectfully traversed.

With respect to claim 1, Liu fails to show, teach, or suggest an application circuit including a mapping driver that maps logical addresses to physical addresses. As best understood by Applicants, Liu discloses mapping logical addresses received from a host to logical addresses of a particular one of a plurality of physical storage devices, but does not disclose mapping logical addresses to physical addresses of any of the physical storage devices.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Liu fails to disclose the limitation that the application circuit includes a mapping driver that maps logical addresses to physical addresses.

As shown in an exemplary embodiment in FIG. 3 of the present invention, an application PCB 130 includes a mapping driver 142 and a buffer 146. The buffer 146 stores application and hard drive related data. The mapping driver 142 is, for example, "a software module that is executed by a processor or hardware module or circuit that performs mapping of logical to physical addresses and/or management of disk drive read/write head location." (Paragraph [0036]). The application PCB 130 sends physical addresses over interfaces 134 and 114 instead of logical addresses. Consequently, it is no longer necessary to include a buffer (and/or a processor as shown in another implementation in FIG. 4A) on an HDA PCB 110.

In contrast, Liu appears to be absent of any teaching or suggestion of an application circuit that maps logical addresses to physical addresses and that transmits the physical addresses. Liu is directed to a storage virtualization computer system that includes a storage virtualization controller (SVC). As shown in FIG. 3, a SVC 200 communicates with a host entity 10 and a physical storage device (PSD) array 400. The SVC 200 "receives IO requests and related data (the control signals and data signals) from the host entity 10 and executes the IO requests internally or maps the IO requests to the PSD array 400." (Paragraph [0045]).

The PSD array 400 includes a plurality of PSDs 420. As best understood by the Applicants, the SVC 200 receives an IO request from the host 10 and maps the IO request to a particular PSD 420 but does not map the IO request to a physical address. For example, the Examiner relies on Paragraphs [0005] and [0010] to disclose this limitation. Paragraph [0005] states that an SVC "is a device the primary purpose of which is to map combinations of sections of physical storage media to logical media units visible to a host system." Similarly, Paragraph [0010] states that the function of an SVC "is to manage, combine, and manipulate physical storage devices in such a way as to present them as a set of logical media units to the host." Applicants respectfully submit that the cited portions of Liu fail to disclose that the SVC 200 maps logical addresses to physical address. Instead, the cited portions disclose that the SVC 200 maps IO requests to individual PSDs 420 in an PSD array 400.

As best understood by the Applicants, the individual PSDs 420 are still required to process the IO requests and map the IO requests to physical addresses. The SVC 200 parses the IO requests and directs them to the corresponding PSD 420 but does not map to, or transmit, physical addresses. For example, Paragraph [0079] recites that the "IO requests are parsed to determine what operation is to be performed and...on which section of the logical media unit the operation is to be performed...appropriate device-side IO requests are generated and issued to the appropriate PSDs 420." Paragraph [0081] states that each IO request includes a "destination media section base address." In other words, the SVC 200 directs the IO requests to the appropriate PSDs 420 but does not map physical addresses.

As noted above, each PSD 420 must still map the IO requests to the proper physical location (i.e. physical address) within the PSD 420. For example, the PSD 420 "parses the request contained in the frame to determine the nature of the operation to be performed and the section of media on which it is to be performed." (Paragraph [0082]). In other words, the PSD 420 parses the request to determine a physical address that corresponds to the request. As such, the SVC 200 does not map logical addresses to physical addresses and does not transmit physical address as claim 1 requires.

Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for similar reasons. Claims 18, 30, 60, 77, 89, 119, 130, and 140, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

REJECTION UNDER 35 U.S.C. § 103

Claims 3 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu in view of Applicants' admission of teaching from prior art, and further in view of Hyde et al. (U.S. Pat. No. 5,751,514).

With respect to independent claim 37, the Examiner alleges that claim 37 is rejected for the same reasons as claim 3. Applicants respectfully note that claim 37 includes limitations that are distinct from claim 3. Claim 37 recites "a first input/output interface that receives data to be stored on the data storage device and data storage device control data including at least one of arm position data and spindle control data from the second I/O interface." Claim 3 does not include this limitation. Further, Applicants respectfully note that the Examiner failed to address similar arguments directed to claim 37 in the response to the Office Action dated December 27, 2005.

Liu fails to show, teach, or suggest the limitation of receiving at least one of arm position data and spindle control data from an application circuit. The Examiner alleges that Liu discloses an application circuit that stores data storage device control data. In particular, the Examiner alleges that the CPC 240 communicates with a non-volatile RAM (NVRAM) 248 that stores storage device control data. For example, Liu states:

> The NVRAM is provided for saving some information regarding the IO operation execution status of the array which can be examined after an abnormal power shut-off occurs in the event that IO operation execution does not complete. (Paragraph [0057]).

The Examiner relies on the "information regarding the IO operation execution status of the array" to disclose "storage device control data." In other words, Liu does not disclose receiving at least one of arm position data and spindle control data from an application circuit. As such, as best understood by Applicants, Liu discloses storing data on the NVRAM but does not disclose receiving arm position data or spindle control data.

Applicants respectfully submit that claim 37 should be allowable for at least the above reasons. Claims 43, 96, 102, 146, 151, 164, and 180 as well as the corresponding dependent claims should be allowable for at least similar reasons.

ALLOWABLE SUBJECT MATTER

The Examiner states that claims 14-15, 55-56, 73-74, 114-115, 126-127, 159-160, 175-176, and 191-192 are allowed. Applicants thank the Examiner for the allowable subject matter.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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